(19)日本国特許庁（ＪＰ）　(12)公開特許公報（A）　(11)特許出願公開番号

特開平6－124231

(43)公開日　平成６年(1994)５月６日

(51)Int.Cl.[5]	識別記号	庁内整理番号	Ｆ Ｉ	技術表示箇所
Ｇ０６Ｆ　12/06	５１０	9366－5B		

審査請求　未請求　請求項の数２(全　５　頁)

(21)出願番号　特願平4－274737

(22)出願日　平成４年(1992)10月14日

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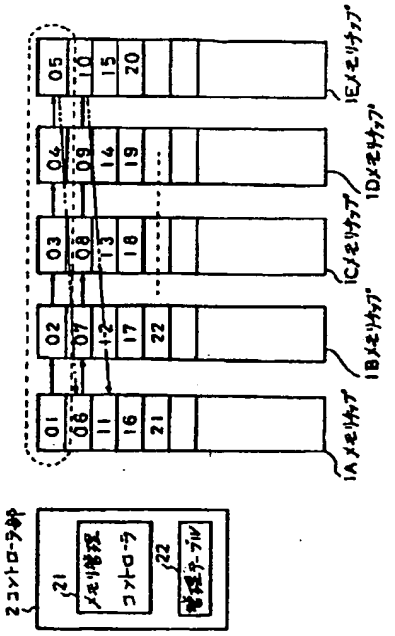
(54)【発明の名称】　半導体ファイル装置

(57)【要約】

【目的】　本発明は、連続したシステム側のブロック番地にデータを書き込む際の時間を短縮化することを目的としている。

【構成】　本発明において、システム側の連続ブロック番地、例えば０１～０５、０６～１０等がメモリチップ１Ａ～１Ｅに跨がって割り付けられているため、コントローラ部２は例えばシステム側の連続ブロック番地０１～０５にデータを書き込む場合、各ブロック番地の存在するメモリチップが異なるため、各ブロック番地に一度にデータを書き込むことができ、データ書き込み速度を高速化している。又、メモリ間に亙って行われるスワッピングの際、メモリ管理コントローラ２１は、当初、メモリチップ１Ａ～１Ｅに跨がって割り付けられたシステム側の連続ブロック番地、例えばブロック番地０１～０５に対応する物理ブロック番地相互間でのみでスワッピングを行うことで、システム側の連続ブロック番地が異なるメモリチップに跨がって割り付けられている状態を維持し、上記効果を保持している。



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1

【特許請求の範囲】

【請求項1】　複数の各メモリチップに内蔵されているフラッシュ型のＥＥＰＲＯＭ内に割り付けられている消去ブロックをシステム側のブロック番地で指定されると、前記消去ブロックにデータを書き込む半導体ファイル装置において、前記システム側のｎ個の連続したブロック番地で指定される前記各消去ブロックが複数の前記メモリチップに１つずつ跨がって配置されるように、前記システム側のブロック番地を前記消去ブロックの物理ブロック番地に変換する変換手段を具備したことを特徴とする半導体ファイル装置。

【請求項2】　複数の各メモリチップに内蔵されているフラッシュ型のＥＥＰＲＯＭ内に割り付けられている消去ブロックをシステム側のブロック番地で指定されると、前記消去ブロックにデータを書き込むと共に、前記各消去ブロックに対するデータの書き込み回数を均等化するためのスワッピングを行う半導体ファイル装置において、前記システム側のｎ個の連続したブロック番地で指定される各消去ブロックが複数の前記メモリチップに１つずつ跨がって配置されるように、前記システム側のブロック番地を前記消去ブロックの物理ブロック番地に変換する変換手段と、別のメモリチップに存在する消去ブロックとの間で行われるスワッピングの際、複数のメモリチップに１つずつ跨がって配置された前記ｎ個のシステム側の連続ブロック番地に対応する前記物理ブロック番地内のみで前記スワッピングを行う制御手段を具備したことを特徴とする半導体ファイル装置。

【発明の詳細な説明】

【０００１】

【産業上の利用分野】本発明は複数のメモリチップを備えた半導体ファイル装置に係わり、特に前記複数のメモリチップ内のフラッシュ型ＥＥＰＲＯＭの消去ブロックにシステム側のブロック番地を割り付ける際の構成に関する。

【０００２】

【従来の技術】従来この種の半導体ファイル装置では複数のメモリチップに内蔵されているフラッシュ型ＥＥＰＲＯＭに割り付けられている消去ブロックが集合されて１つの大きなメモリ領域が構成されている。コントローラはシステム側からデータの書き込み先のブロック番地を受け取ると、これを前記メモリチップ側の物理ブロック番地に変換して、データを書き込む制御を行う。従って、コントローラはシステム側のブロック番地をメモリチップ側の物理ブロック番地に変換する機能を有している。

【０００３】図３は上記のような複数のメモリチップ１Ａ～１Ｃにより構成されるメモリ領域を示したもので、各メモリチップを区画している枠は消去ブロックを示しているものとする。ここで、上記システム側のブロック番地０１～１４を図に示したようにメモリチップ１Ａに

2

割り付け、メモリチップ１Ｂにブロック番地１５～２８を割り付け、メモリチップ１Ｃにブロック番地２９～４２を割り付けたとする。このようにシステム側のブロック番地をメモリチップの消去ブロックに割り付けた構成にて、連続したシステム側のブロック番地０１、０２、０３に上記コントローラがデータの書き込みを行う場合、１つのメモリチップ内にある複数の消去ブロックへのデータの書き込みは逐次行わなければならない。このため、コントローラは、まず、ブロック番地０１にデータを書き込んだ後、次のブロック番地０２にデータを書き込み、更にブロック番地０３にデータを書き込まなければならず、データの書き込みに時間がかかってしまうという欠点があった。尚、従来から異なるメモリチップ内にあるそれぞれの消去ブロックには同時にデータを書き込むことができるようになっている。

【０００４】

【発明が解決しようとする課題】複数のメモリチップを有する半導体ファイル装置にて、システム側のブロック番地を前記メモリチップの各消去ブロックに無作為に割り付けると、例えば連続したシステム側のブロック番地にデータを書き込む際に、連続したシステム側のブロック番地が１つのメモリチップ内に集中してしまうことが生じ、前記データの書き込みに時間がかかってしまうという欠点があった。

【０００５】そこで本発明は上記の欠点を除去し、連続したシステム側のブロック番地にデータを書き込む際の時間を短縮化することができる半導体ファイル装置を提供することを目的としている。

【０００６】

【課題を解決するための手段】本発明は複数の各メモリチップに内蔵されているフラッシュ型のＥＥＰＲＯＭ内に割り付けられている消去ブロックをシステム側のブロック番地で指定されると、前記消去ブロックにデータを書き込むと共に、前記各消去ブロックに対するデータの書き込み回数を均等化するためのスワッピングを行う半導体ファイル装置において、前記システム側のｎ個の連続したブロック番地で指定される各消去ブロックが複数の前記メモリチップに１つずつ跨がって配置されるように、前記システム側のブロック番地を前記消去ブロックの物理ブロック番地に変換する変換手段と、別のメモリチップに存在する消去ブロックとの間で行われるスワッピングの際、複数のメモリチップに１つずつ跨がって配置された前記ｎ個のシステム側の連続ブロック番地に対応する前記物理ブロック番地内のみで前記スワッピングを行う制御手段を具備した構成を有する。

【０００７】

【作用】本発明の半導体ファイル装置において、変換手段はシステム側のｎ個の連続したブロック番地で指定される各消去ブロックが複数のメモリチップに１つずつ跨がって配置されるように、前記システム側のブロック番

3

地を前記消去ブロックの物理ブロック番地に変換する。制御手段は別のメモリチップに存在する消去ブロックとの間で行われるスワッピングの際、複数のメモリチップに1つずつ跨がって配置された前記n個のシステム側の連続ブロック番地に対応する前記物理ブロック番地内のみで前記スワッピングを行う。

【0008】

【実施例】以下、本発明の一実施例を図面を参照して説明する。図1は本発明の半導体ファイル装置の一実施例を示したブロック図である。1A～1Eは本半導体ファイル装置のメモリ領域を構成するメモリチップで、各メモリチップはフラッシュ型EEPROMを構成しているものとし、図中、各メモリチップを区画した1枠は1消去ブロックを示しているものとする。2は上記メモリチップ1A～1Eへのデータの読み書き制御を行うコントローラ部で、システム側のブロック番地をメモリチップ側の物理ブロック番地に変換するメモリ管理コントローラ21及び前記変換時に必要なシステム側のブロック番地とメモリチップ側の物理ブロック番地との対応関係データを格納している管理テーブル22を有している。

【0009】次に本実施例の動作について説明する。コントローラ部2の管理テーブル22にはシステム側の連続番地が1つのメモリチップに集中することなく、メモリチップ1A～1Eに1個ずつできるだけ分散するように、前記システム側のブロック番地を各メモリチップの消去ブロックに割り付ける変換データが格納されている。即ち、システム側のブロック番地01～05はそれぞれ1個ずつメモリチップ1A～1Eの消去ブロックに分散して割り付けられ、システム側のブロック番地06～10も同様にメモリチップ1A～1Eの消去ブロックに分散して割り付けられており、以下に続くシステム側の連続したブロック番地も同様である。

【0010】コントローラ部2は例えば図示されないシステム側からブロック番地01～05の連続したブロックへのデータの書き込み指令を受けると、メモリ管理コントローラ21が管理テーブル22を参照して、前記システム側のブロック番地をメモリチップ1A～1E内の物理ブロック番地に変換し、得られた物理ブロック番地にデータの書き込みを行う。本例では、前記システム側のブロック番地01～05は図示の如くメモリチップ1A～1Eの各消去ブロックに1個ずつ跨がって割り付けられているため、コントローラ部2は各メモリチップ1A～1E上の前記ブロック番地01～05へのデータの書き込みを一度に行って処理を終了する。しかし、上記システム側のブロック番地01～05が1つのメモリチップ上に割り付けられていたとすれば、コントローラ部2はこれら各ブロック番地へのデータの書き込みを逐次行わなければならず、上記本例の場合に比べて5倍の書き込み時間を要することになる。

【0011】次に、コントローラ部2がブロック番地01～08の連続したブロックにデータを書き込む場合、各ブロック番地はメモリチップ1A～1Eに分散して割り付けられているが、ブロック番地01と06は同一メモリチップ1Aに割り付けられ、ブロック番地02と07は同一メモリチップ1Bに割り付けられ、更にブロック番地03と08は同一メモリチップ1Cに割り付けられている。このため、コントローラ部2は、まず、メモリチップ1A～1Eに割り付けられているブロック番地01～05に同時にデータを書き込んだ後、メモリチップ1A～1Cに割り付けられているブロック番地06～08にデータを書き込んで、処理を終了する。この例では、上記した例に比べて、2倍ほど書き込み時間がかかるが、例えばシステム側のブロック番地が図3に示したように各メモリチップへ割り付けてあるような従来例に比べて、データの書き込み時間を2／8に短縮化することができる。

4

【0012】ところで、上記のようにメモリチップ1A～1Eに内蔵されているメモリの種類が、フラッシュ型EEPROMであった場合、各フラッシュ型EEPROM内の物理番地の使用頻度が均一になるように、スワッピング処理が行われる。従って、このスワッピング処理が行われると、システム側のブロック番地とメモリチップ側の物理ブロック番地との対応関係が異なってしまい、当初、図1に示すようにシステム側のブロック番地を各メモリチップ上の消去ブロックに割り付けても、この割り付けが崩れて、例えばシステム側のブロック番地01とブロック番地02とブロック番地03が同一のメモリチップ1A内に割り付けられてしまうというようなことが起きる可能性がある。そこで本例では、当初図1の如くメモリチップ1A～1Eに1番地ずつ跨がって割り付けたシステム側のブロック番地01～05や06～10や11～15…が同じメモリチップ内に割り付けられることがないように、スワッピングをしなければならない。そこで、ルール（1）として、システム側から見たブロック番地が横断的に格納されている図1の点線に示すような仮想横断位置内の同じグループに入るメモリチップ上の物理ブロック番地同志でしか、異なるメモリチップ間に跨がるスワッピングを認めないようにすれば、上記した当初の設定を崩すことがなくなる。又、ルール（2）として、同一メモリチップ内の物理ブロック番地同志ではスワッピングを認めても、上記した当初の設定を崩すことがない。

【0013】図2は上記のルール（1）、（2）でスワッピングを行った場合の、メモリチップ1A～1Eに対するシステム側のブロック番地の再割り付け例を示した図である。この例では、メモリチップ1Aのブロック番地01とメモリチップ1Bのブロック番地02とをスワッピングにより交換した後、更にメモリチップ1B内のブロック番地01と07をスワッピングにより交換することにより、図の如くシステム側のブロック番地がメモ

5

リチップ上に再配置されることになる。この例にてブロック番地０１～０５のグループを見てみると各ブロック番地はメモリチップ１Ａ～１Ｅに１番地ずつ分散して配置されている。又、ブロック番地０６～１０のグループを見てみると、各ブロック番地はメモリチップ１Ａ～１Ｅに同様に分散しており、上記した当初の設定が崩れていないことが分かる。従って、コントローラ部２のメモリ管理コントローラ２１はスワッピングが必要になった場合、上記したルールに従ってメモリチップ１Ａ～１Ｅの物理ブロック番地のスワッピングを行うため、連続したシステム側の複数のブロック番地に対するデータの書き込みを短時間化できる特性はスワッピング後も保持される。

【００１４】本実施例によれば、システム側のブロック番地をメモリチップ１Ａ～１Ｅの消去ブロックに割り付ける際に、システム側の連続したブロック番地がメモリチップ１Ａ～１Ｅに１番地ずつ跨がって配置されるように、即ち、連続したブロック番地が同一のメモリチップ内にできるだけ割り付けられないように配置することにより、連続した消去ブロック間に跨がるデータの書き込みが生じた場合、上記した各メモリチップに分散されている前記連続したブロックに同時にデータを書き込むことができ、この種のデータの書き込み処理時間を短縮化することができる。又、当初メモリチップ１Ａ～１Ｅに分散して割り付けたシステム側のブロック番地に対応する

6

物理ブロック番地同志内でのみ、スワッピングを行うようにし、且つ同一メモリチップ内の前記ブロック番地に関しては自由にスワッピングを行う規定を設けることにより、スワッピング後も連続したシステム側のブロック番地がメモリチップ１Ａ～１Ｅに分散した形態を保持することができ、上記効果が減殺されるのを防止することができる。

【００１５】

【発明の効果】以上記述した如く本発明の半導体ファイル装置によれば、連続したシステム側のブロック番地にデータを書き込む際の時間を短縮化することができる。

【図面の簡単な説明】

【図１】本発明の半導体ファイル装置の一実施例を示したブロック図。

【図２】図１の装置でスワッピングを行った場合の、複数のメモリチップの消去ブロックに対するシステム側のブロック番地の再割り付け例を示した図。

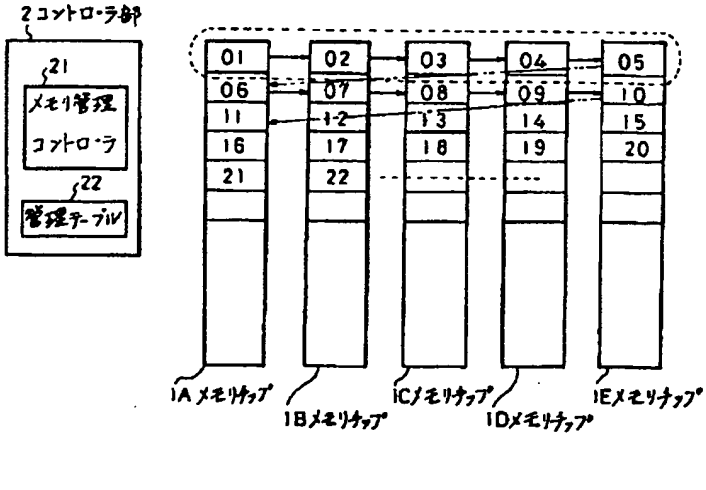
【図３】従来のシステム側のブロック番地を複数のメモリチップ間の消去ブロックに割り付けた例を示した図。

【符号の説明】

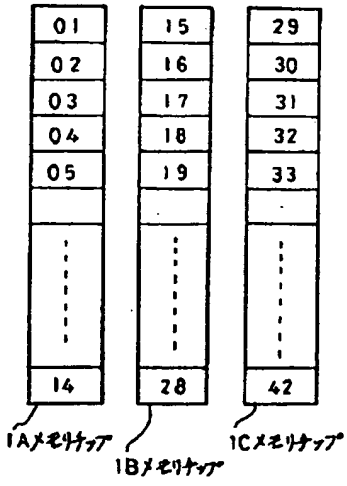
１Ａ～１Ｅ…メモリチップ　　２…コントローラ部

２１…メモリ管理コントローラ　　２２…管理テーブル

【図１】



【図３】



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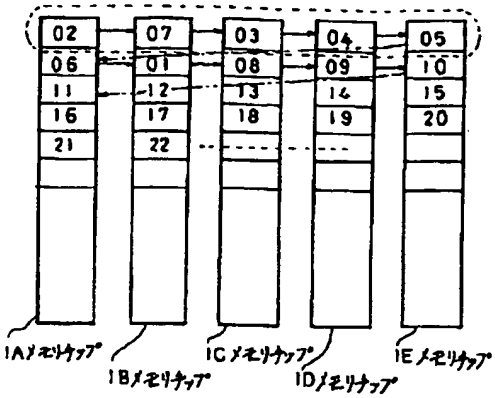
【図2】


02
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1Aメモリチップ
1Bメモリチップ
1Cメモリチップ
1Dメモリチップ
1Eメモリチップ

Japanese Patent Laid-Open No. 124231/1994

Laid-Open Date: May 6, 1994

Application Date: October 14, 1992

Applicant: Toshiba Corporation

Title:

SEMICONDUCTOR FILING DEVICE

Abstract:

[Purpose] To reduce the time required for writing data at the consecutive block addresses of the system side.

[Constitution] In the invention, the consecutive block addresses, for example, 01 to 05, 06 to 10 are allocated extending over memory chips 1A to 1E, whereby when the controller part 2 writes data at the consecutive block addresses 01 to 05 of the system side, the respective block addresses exist in different memory chips, so the data can be written at the respective block addresses at the same time so as to attain high speed data writing. In swapping executed between memories, a memory management controller 21 first executes swapping only between the mutual physical block addresses corresponding to the consecutive block addresses of the system side allocated extending over the memory chips 1A to 1E such as the block addresses 01 to 05, whereby the state where the consecutive block addresses of the system side are allocated extending over the different memory chips is kept to maintain the above effect.

Claims:

1. A semiconductor filing device, in which when a plurality of erasure blocks allocated to flash EEPROMs housed in the respective memory chips are assigned to the block addresses of the system side, data is written to the erasure blocks, characterized in that the semiconductor filing device comprises: converting means for converting the block address of the system side to a physical block address of the erasure block so that the erasure blocks assigned to n-number of consecutive block addresses are disposed extending over a plurality of memory chips, the next block being on the next chip.

2. A semiconductor filing device, in which when a plurality of erasure blocks allocated to flash EEPROMs housed in the respective memory chips are assigned to the block addresses of the system side, data is written to the erasure blocks, and swapping is performed for equalizing the number of times data is written to the respective erasure blocks, characterized in that the semiconductor filing device comprises: converting means for converting the block address of the system side to a physical block address of the erasure block so that the erasure blocks assigned to n-number of consecutive block addresses are disposed extending over a plurality of memory chips, the next block being on the next chip; and control means for performing swapping only among the physical block addresses corresponding

to the n-number of consecutive block addresses of the system side disposed extending over the plurality of memory chip, the next block being on the next chip, in swapping performed between the erasure blocks existing in different memory chips.

Detailed Description of the Invention:

[0001]

[Industrial Field of Application]

This invention relates to a semiconductor filing device having a plurality of memory chips and particularly to the constitution allocating block addresses of the system side to the erasure blocks of the flash EEPROMs in the plurality of memory chips.

[0002]

[Prior Art]

In the conventional semiconductor filing device of this type, erasure blocks allocated to the flash EEPROMs housed in the plurality of memory chips are assembled to form one large memory area. On receiving the block address of a data writing destination from the system side, a controller conducts the control for converting the address to a physical block address of the memory chip side and writing data. Accordingly, the controller has the function of converting the block address of the system side to the physical block address of the memory side.

[0003]

Fig. 3 is a diagram showing memory areas constituted by a plurality of memory chips 1A to 1C described above, in which frames dividing the respective memory chips indicate erase blocks. In this arrangement, the block numbers 01 to 14 are, as shown in the drawing, allocated to the memory chip 1A, the block addresses 15 to 28 are allocated to the memory chip 1B, and the block addresses 29 to 42 are allocated to the memory chip 1C. In the case where the controller writes data to the consecutive block addresses 01, 02, 03 of the system side in the constitution where the block addresses of the system side are allocated to the erasure blocks, it is necessary to sequentially perform writing of data to the plurality of erasure blocks in one memory chip. Therefore, the controller has to first write data at the block address 01, then write data at the next block address 02, and further write data at the block address 03, resulting in the disadvantage that it takes much time to write data. It has however been possible to simultaneously write data to blocks existing in different memory chips.

[0004]

[Problems that the Invention to Solve]

In a semiconductor filing device having a plurality of memory chips, when the block addresses of the system side are allocated to the respective erasure blocks of the plurality

of memory chips at random, in the case of writing data to the consecutive block addresses of the system side, the consecutive block addresses of the system side are concentrated in one memory chip, resulting in the disadvantage that it takes much time to write the data.

[0005]

It is, accordingly, an object of the invention to overcome the above disadvantage and provide a semiconductor filing device capable of reducing the time required for writing data to the consecutive block addresses of the system side.

[0006]

[Means for Solving the Problems]

According to the invention, a semiconductor filing device, in which when a plurality of erasure blocks allocated to flash EEPROMs housed in the respective memory chips are assigned to the block addresses of the system side, data is written to the erasure blocks, and swapping is performed for equalizing the number of times data is written to the respective erasure blocks, includes: converting means for converting the block address of the system side to a physical block address of the erasure block so that the erasure blocks assigned to n-number of consecutive block addresses are disposed extending over a plurality of memory chips, the next block being on the next chip; and control means for performing swapping only aamong the physical block addresses corresponding to the n-number of

consecutive block addresses of the system side disposed extending over the plurality of memory chips, the next block being on the next chip, in swapping performed between the erasure blocks existing in different memory chips.

[0007]

[Operation]

In the semiconductor filing device of the invention, the converting means converts the block addresses of the system side to the physical block addresses of the erasure blocks so that the respective erasure blocks assigned to n-number of consecutive block addresses of the system side are disposed extending over the plurality of memory chips, the next block being on the next chip. The control means performs swapping only among the physical block addresses corresponding to n-number of consecutive block addresses of the system side disposed extending over the plurality of memory chips, the next block being on the next chip, in swapping performed between the erasure blocks existing in different memory chips.

[0008]

[Embodiment]

One embodiment of the invention will now be described with reference to the attached drawings. Fig. 1 is a block diagram showing one embodiment of a semiconductor filing device according to the invention. The reference numerals 1A to 1E are memory chips constituting the memory area of the

semiconductor filing device, and each memory chip constitutes a flash EEPROM. In the drawing, one divided frame of each memory chip indicates one erasure block. The reference numeral 2 designates a controller part for conducting the control for reading and writing data to the memory chips 1A to 1E, which has a memory management controller 21 for converting the block address of the system side to the physical block address of the memory chip side, and a management table 22 storing the data on the correspondence between the block address of the system side and the physical block address of the memory chip side required for the above conversions.

[0009]

The operation of the embodiment will now be described. The management table 22 of the controller part 2 stores the conversion data for allocating the block addresses of the system sides to the erasure blocks of the respective memory chips so that the consecutive addresses of the system side are dispersed to the memory chips 1A to 1E without being concentrated in one memory chip, the next block being on the next chip or as close to that as possible. That is, the block addresses 01 to 05 of the system side are dispersed and allocated respectively to the erasure blocks of the memory chips 1A to 1E, and the block addresses 06 to 10 of the system side are similarly dispersed and allocated to the erase blocks of the memory chips 1A to 1E. The subsequent consecutive block addresses of the

system side are handled similarly.

[0010]

In the controller part 2, on receiving a command for writing data to the consecutive blocks at block addresses 01 to 05 from the system side not shown, the memory management controller 21 converts the block addresses of the system side to the physical block addresses in the memory chips 1A to 1E with reference to the management table 22, and writes the data at the obtained physical block addresses. In the present embodiment, the block addresses 01 to 05 of the system side are, as shown in the drawing, allocated extending over the respective erasure blocks of the memory chips 1A to 1E, the next block being on the next chip, and the controller part 2 ends the processing by writing data at the block addresses 01 to 05 on the respective memory chips 1A to 1E all at once. If the block addresses 01 to 05 of the system side had been allocated to one memory chip, however, the controller part 2 would have to write data to the respective block addresses one by one, so that it requires five times as much writing time as the present embodiment.

[0011]

In the case where the controller part 2 writes data to the consecutive blocks at the block addresses 01 to 08, although the respective block addresses are dispersed and allocated to the memory chips 1A to 1E, the block addresses 01 and 06 are allocated to the same memory chip 1A, the block addresses 02

and 07 are allocated to the same memory chip 1B, and further the block addresses 03 and 08 are allocated to the same memory chip 1C. Therefore, the controller part 2 first writes data to the block addresses 01 to 05 allocated to the memory chips 1A to 1E at the same time, and then writes data to the block addresses 06 to 08 allocated to the memory chips 1A to 1C to end the processing. In this example, the write time is twice as much as that in the above example, but as compared with the conventional case where the block addresses of the system side are, as shown in Fig. 3, allocated to the respective memory chips, for example, the data write time can be reduced to 2/8. [0012]

In the case where the type of the memories housed in the memory chips 1A to 1E is the flash EEPROM, swapping process is performed so that the use frequency of physical addresses in the respective flash EEPROMs is uniform. Accordingly, when the swapping process is performed, the relationship of correspondence between the block address of the system side and the physical block address of the memory chip side is varied, so there is the possibility that even if the block addresses of the system side are, as shown in Fig. 1, allocated to the erasure block of each memory chip at the beginning, the allocation is changed, so that the block address 01, the block address 02 and the block address 03 of the system side are allocated to the same memory chip 1A. Then, in this example,

it is necessary to perform swapping so that the block addresses of each group 01 to 05, 06 to 10, or 11 to 15 ... of the system side are allocated extending over all the memory chips 1A to 1E at the beginning as shown in Fig. 1 are not thereafter allocated to the same memory chip. When it is made a rule (1) that swapping between different memory chips is permitted only among the physical block addresses on the memory chips of the same group crossing horizontally as shown by the dotted line in Fig. 1 where the block addresses seen from the system side are stored transversely, the above initial setting is not broken. When it is made a rule (2) that swapping is also permitted between the physical blocks addresses in the same memory chip, the above initial setting is not broken.

[0013]

Fig. 2 is a diagram showing an example where the block addresses of the system side are re-allocated to the memory chips 1A to 1E in the case of performing swapping according to the rules (1), (2). In this example, after the block address 01 of the memory chip 1A is exchanged with the block address 02 of the memory chip 1B by swapping, the block addresses 01 and 07 in the memory chip 1B are then exchanged with each other by swapping, thereby relocating the block addresses of the system side on the memory chips as shown in the drawing. In this example, looking at the group of the block addresses 01 to 05, the respective block addresses are dispersed and disposed one by

one in the memory chips 1A to 1E. Looking at the group of the block addresses 06 to 10, the respective block addresses are similarly dispersed in the memory chips 1A to 1E. It is thus evident that the initial setting is not broken. Accordingly, the memory management controller 21 of the controller part 2 performs swapping at the physical block addresses of the memory chips 1A to 1E according to the above rules when swapping is needed, whereby the characteristic of reduced time for writing data to the plurality of consecutive block addresses can be kept after swapping.

[0014]

According to the present embodiment, the block addresses of the system side are allocated to the erasure blocks of the memory chips 1A to 1E so that the consecutive block addresses of the system side are disposed extending over the memory chips 1A to 1E the next block being on the next chip; that is, the consecutive block addresses are not allocated in the same memory chip as much as possible, whereby when writing of data extending over the consecutive erasure blocks occurs, the data can be simultaneously written to the consecutive blocks dispersed to the above respective memory chips so that the processing time for writing the data of this type can be reduced. The rules that swapping is performed only among the physical block addresses corresponding to the block addresses of the system side dispersed and allocated to the memory chips 1A to 1E at

the beginning, and that swapping is freely performed among the block addresses in the same memory chip, are provided to thereby keep the form where the consecutive block addresses of the system side are dispersed in the memory chips 1A to 1E even after swapping, whereby the above effect can be prevented from being lessened.

[0015]

[Effect of the Invention]

According to the invention, as described above, the semiconductor filing device can reduce the time required for writing data in the consecutive block addresses of the system side.

Brief Description of the Drawings:

Fig. 1 is a block diagram showing one embodiment of a semiconductor filing apparatus according to the invention; and

Fig. 2 is a diagram showing an example of re-allocating the block addresses of the system side to the erasure blocks of a plurality of memory chips in the case of performing swapping in the apparatus of Fig. 1; and

Fig. 3 is a diagram showing an example of allocating the block addresses of the system side to the erasure blocks of a plurality of memory chips according to the prior art.

[Description of the Reference Numerals and Signs]

1A to 1E: memory chip 2: controller part 21: memory management controller 22: management table

FIGURE 1:

2: CONTROLLER PART 21: MEMORY MANAGEMENT CONTROLLER 22: MANAGEMENT TABLE

1A to 1E: MEMORY CHIP

FIGURE 2:

1A to 1E: MEMORY CHIP

FIGURE 3:

1A to 1C: MEMORY CHIP

AMENDMENT

[Date of Submission] June 18, 1998

[Amendment 1]

[Object of Amendment Document Name] Specification

[Object of Amendment Item Name] Title of the Invention

[Method of Amendment] Change

[Contents of Amendment]

Title of the Invention:

CONTROL METHOD FOR SEMICONDUCTOR MEMORY DEVICE

[Amendment 2]

[Object of Amendment Document Name] Specification

[Object of Amendment Item Name] Claims

[Method of Amendment] Change

[Contents of Amendment]

FH 008605

Claims:

1. A control method for a semiconductor memory device, in which in a semiconductor memory device having a plurality of memory chips to which a plurality of blocks are allocated, to the blocks are designated block addresses of the system side and data is written to the blocks, characterized in that the block address of the system side is converted to the physical block address of the block so that the respective blocks assigned

to the consecutive block addresses of the system side are disposed extending over the plurality of memory chips, the next block being on the next chip.

2. A control method for a semiconductor memory device, in which in a semiconductor memory device having a plurality of memory chips to which a plurality of blocks are allocated, to the blocks are designated block addresses of the system side, data is written to the blocks, and swapping is performed for equalizing the number of times data is written to the respective blocks, characterized in that the block address of the system side is converted to the physical block address of the block so that the respective blocks assigned to the consecutive block addresses of the system side are disposed extending over the plurality of memory the next block being on the next chip, and in swapping between the blocks existing in different memory chips, the swapping is performed only among the physical block addresses corresponding to the consecutive block addresses of the system side disposed extending over the plurality of memory chips one block for each chip.

[Amendment 3]

[Object of Amendment Document Name] Specification

[Object of Amendment Item Name] 0005

[Method of Amendment] Change

[Contents of Amendment]

[0005] It is an object of the invention to overcome the above disadvantage and provide a control method for a semiconductor memory device which may reduce the time required for writing to a semiconductor memory device the data corresponding to the consecutive block addresses of the system side and provide a control method for a semiconductor memory device which may equalize the use frequency of the respective block addresses in a memory module while reducing the time required for writing data.

[Amendment 4]

[Object of Amendment Document Name] Specification

[Object of Amendment Item Name] 0006

[Method of Amendment] Change

[Contents of Amendment]

FH 008607

[0006] According to the invention, in a control method for a semiconductor memory device in which a semiconductor memory device has a plurality of memory chips to each of which a plurality of blocks are allocated and data is written to the blocks when block addresses are designated by a host device, the block addresses of the system side are converted to the physical block addresses of the blocks in such a way that the respective blocks assigned to the consecutive block addresses of the system side are disposed extending over the plurality of memory chips the next block being on the next chip. Further, according to the

invention, in a control method for a semiconductor memory device in which a semiconductor memory device has a plurality of memory chips to each of which a plurality of blocks are allocated and data is written to the blocks when block addresses on the system side are designated, and swapping is performed for equalizing the number if times data is written to the respective blocks, the block address of the system side is converted to the physical block address of the block so that the respective blocks assigned to the consecutive block addresses of the system side are disposed extending over the plurality of memory chips, the next block being on the next chip, and in swapping between the blocks existing in different memory chips, the swapping is performed only at the physical block addresses corresponding to the consecutive block addresses of the host side disposed extending over the plurality of memory chips, the next block being on the next chip.

[Amendment 5]

[Object of Amendment Document Name] Specification

[Object of Amendment Item Name] 0007

[Method of Amendment] Change

[Contents of Amendment]

[0007]

[Operation]

FH 008608

In the control method for the semiconductor memory device

of the invention, the block address of the system is converted to the physical block address of the block of the semiconductor memory device so that the respective blocks of the semiconductor memory device assigned to the consecutive block addresses of the system side are disposed extending over the plurality of memory chips, the next block being on the next chip. In swapping between the blocks existing in different memory chips, the swapping is performed only at the physical block addresses corresponding to the consecutive block addresses of the system side disposed extending over the plurality of memory chips, the next block being on the next chip.

[Amendment 6]

[Object of Amendment Document Name] Specification

[Object of Amendment Item Name] 0015

[Method of Amendment] Change

[Contents of Amendment]

[0015]

[Effect of the Invention]

According to the invention, as described above, in the control method for the semiconductor memory device, the time required for writing data at the consecutive block addresses of the system side can be reduced. While the time for writing data is reduced, the use frequency of the respective block addresses in the memory module can be equalized.

Japanese Patent Laid-Open No. 124231/1994

Laid-Open Date: May 6, 1994

Application Date: October 14, 1992

Applicant: Toshiba Corporation

Title:

SEMICONDUCTOR FILING DEVICE

Abstract:

[Purpose] To reduce the time required for writing data at the consecutive block addresses of the system side.

[Constitution] In the invention, the consecutive block addresses, for example, 01 to 05, 06 to 10 are allocated extending over memory chips 1A to 1E, whereby when the controller part 2 writes data at the consecutive block addresses 01 to 05 of the system side, the respective block addresses exist in different memory chips, so the data can be written at the respective block addresses at the same time so as to attain high speed data writing. In swapping executed between memories, a memory management controller 21 first executes swapping only between the mutual physical block addresses corresponding to the consecutive block addresses of the system side allocated extending over the memory chips 1A to 1E such as the block addresses 01 to 05, whereby the state where the consecutive block addresses of the system side are allocated extending over the different memory chips is kept to maintain the above effect.

Claims:

1. A semiconductor filing device, in which when a plurality of erasure blocks allocated to flash EEPROMs housed in the respective memory chips are assigned to the block addresses of the system side, data is written to the erasure blocks, characterized in that the semiconductor filing device comprises: converting means for converting the block address of the system side to a physical block address of the erasure block so that the erasure blocks assigned to n-number of consecutive block addresses are disposed extending over a plurality of memory chips, the next block being on the next chip.

2. A semiconductor filing device, in which when a plurality of erasure blocks allocated to flash EEPROMs housed in the respective memory chips are assigned to the block addresses of the system side, data is written to the erasure blocks, and swapping is performed for equalizing the number of times data is written to the respective erasure blocks, characterized in that the semiconductor filing device comprises: converting means for converting the block address of the system side to a physical block address of the erasure block so that the erasure blocks assigned to n-number of consecutive block addresses are disposed extending over a plurality of memory chips, the next block being on the next chip; and control means for performing swapping only among the physical block addresses corresponding

to the n-number of consecutive block addresses of the system side disposed extending over the plurality of memory chip, the next block being on the next chip, in swapping performed between the erasure blocks existing in different memory chips.

Detailed Description of the Invention:

[0001]

[Industrial Field of Application]

This invention relates to a semiconductor filing device having a plurality of memory chips and particularly to the constitution allocating block addresses of the system side to the erasure blocks of the flash EEPROMs in the plurality of memory chips.

[0002]

[Prior Art]

In the conventional semiconductor filing device of this type, erasure blocks allocated to the flash EEPROMs housed in the plurality of memory chips are assembled to form one large memory area. On receiving the block address of a data writing destination from the system side, a controller conducts the control for converting the address to a physical block address of the memory chip side and writing data. Accordingly, the controller has the function of converting the block address of the system side to the physical block address of the memory side.

[0003]

Fig. 3 is a diagram showing memory areas constituted by a plurality of memory chips 1A to 1C described above, in which frames dividing the respective memory chips indicate erase blocks. In this arrangement, the block numbers 01 to 14 are, as shown in the drawing, allocated to the memory chip 1A, the block addresses 15 to 28 are allocated to the memory chip 1B, and the block addresses 29 to 42 are allocated to the memory chip 1C. In the case where the controller writes data to the consecutive block addresses 01, 02, 03 of the system side in the constitution where the block addresses of the system side are allocated to the erasure blocks, it is necessary to sequentially perform writing of data to the plurality of erasure blocks in one memory chip. Therefore, the controller has to first write data at the block address 01, then write data at the next block address 02, and further write data at the block address 03, resulting in the disadvantage that it takes much time to write data. It has however been possible to simultaneously write data to blocks existing in different memory chips.

[0004]

[Problems that the Invention to Solve]

In a semiconductor filing device having a plurality of memory chips, when the block addresses of the system side are allocated to the respective erasure blocks of the plurality

of memory chips at random, in the case of writing data to the consecutive block addresses of the system side, the consecutive block addresses of the system side are concentrated in one memory chip, resulting in the disadvantage that it takes much time to write the data.

[0005]

It is, accordingly, an object of the invention to overcome the above disadvantage and provide a semiconductor filing device capable of reducing the time required for writing data to the consecutive block addresses of the system side.

[0006]

[Means for Solving the Problems]

According to the invention, a semiconductor filing device, in which when a plurality of erasure blocks allocated to flash EEPROMs housed in the respective memory chips are assigned to the block addresses of the system side, data is written to the erasure blocks, and swapping is performed for equalizing the number of times data is written to the respective erasure blocks, includes: converting means for converting the block address of the system side to a physical block address of the erasure block so that the erasure blocks assigned to n-number of consecutive block addresses are disposed extending over a plurality of memory chips, the next block being on the next chip; and control means for performing swapping only aamong the physical block addresses corresponding to the n-number of

consecutive block addresses of the system side disposed extending over the plurality of memory chips, the next block being on the next chip, in swapping performed between the erasure blocks existing in different memory chips.

[0007]

[Operation]

In the semiconductor filing device of the invention, the converting means converts the block addresses of the system side to the physical block addresses of the erasure blocks so that the respective erasure blocks assigned to n-number of consecutive block addresses of the system side are disposed extending over the plurality of memory chips, the next block being on the next chip. The control means performs swapping only among the physical block addresses corresponding to n-number of consecutive block addresses of the system side disposed extending over the plurality of memory chips, the next block being on the next chip, in swapping performed between the erasure blocks existing in different memory chips.

[0008]

[Embodiment]

One embodiment of the invention will now be described with reference to the attached drawings. Fig. 1 is a block diagram showing one embodiment of a semiconductor filing device according to the invention. The reference numerals 1A to 1E are memory chips constituting the memory area of the

semiconductor filing device, and each memory chip constitutes a flash EEPROM. In the drawing, one divided frame of each memory chip indicates one erasure block. The reference numeral 2 designates a controller part for conducting the control for reading and writing data to the memory chips 1A to 1E, which has a memory management controller 21 for converting the block address of the system side to the physical block address of the memory chip side, and a management table 22 storing the data on the correspondence between the block address of the system side and the physical block address of the memory chip side required for the above conversions.

[0009]

The operation of the embodiment will now be described. The management table 22 of the controller part 2 stores the conversion data for allocating the block addresses of the system sides to the erasure blocks of the respective memory chips so that the consecutive addresses of the system side are dispersed to the memory chips 1A to 1E without being concentrated in one memory chip, the next block being on the next chip or as close to that as possible. That is, the block addresses 01 to 05 of the system side are dispersed and allocated respectively to the erasure blocks of the memory chips 1A to 1E, and the block addresses 06 to 10 of the system side are similarly dispersed and allocated to the erase blocks of the memory chips 1A to 1E. The subsequent consecutive block addresses of the

system side are handled similarly.

[0010]

In the controller part 2, on receiving a command for writing data to the consecutive blocks at block addresses 01 to 05 from the system side not shown, the memory management controller 21 converts the block addresses of the system side to the physical block addresses in the memory chips 1A to 1E with reference to the management table 22, and writes the data at the obtained physical block addresses. In the present embodiment, the block addresses 01 to 05 of the system side are, as shown in the drawing, allocated extending over the respective erasure blocks of the memory chips 1A to 1E, the next block being on the next chip, and the controller part 2 ends the processing by writing data at the block addresses 01 to 05 on the respective memory chips 1A to 1E all at once. If the block addresses 01 to 05 of the system side had been allocated to one memory chip, however, the controller part 2 would have to write data to the respective block addresses one by one, so that it requires five times as much writing time as the present embodiment.

[0011]

In the case where the controller part 2 writes data to the consecutive blocks at the block addresses 01 to 08, although the respective block addresses are dispersed and allocated to the memory chips 1A to 1E, the block addresses 01 and 06 are allocated to the same memory chip 1A, the block addresses 02

and 07 are allocated to the same memory chip 1B, and further the block addresses 03 and 08 are allocated to the same memory chip 1C. Therefore, the controller part 2 first writes data to the block addresses 01 to 05 allocated to the memory chips 1A to 1E at the same time, and then writes data to the block addresses 06 to 08 allocated to the memory chips 1A to 1C to end the processing. In this example, the write time is twice as much as that in the above example, but as compared with the conventional case where the block addresses of the system side are, as shown in Fig. 3, allocated to the respective memory chips, for example, the data write time can be reduced to 2/8.

[0012]

In the case where the type of the memories housed in the memory chips 1A to 1E is the flash EEPROM, swapping process is performed so that the use frequency of physical addresses in the respective flash EEPROMs is uniform. Accordingly, when the swapping process is performed, the relationship of correspondence between the block address of the system side and the physical block address of the memory chip side is varied, so there is the possibility that even if the block addresses of the system side are, as shown in Fig. 1, allocated to the erasure block of each memory chip at the beginning, the allocation is changed, so that the block address 01, the block address 02 and the block address 03 of the system side are allocated to the same memory chip 1A. Then, in this example,

it is necessary to perform swapping so that the block addresses of each group 01 to 05, 06 to 10, or 11 to 15 ... of the system side are allocated extending over all the memory chips 1A to 1E at the beginning as shown in Fig. 1 are not thereafter allocated to the same memory chip. When it is made a rule (1) that swapping between different memory chips is permitted only among the physical block addresses on the memory chips of the same group crossing horizontally as shown by the dotted line in Fig. 1 where the block addresses seen from the system side are stored transversely, the above initial setting is not broken. When it is made a rule (2) that swapping is also permitted between the physical blocks addresses in the same memory chip, the above initial setting is not broken.

[0013]

Fig. 2 is a diagram showing an example where the block addresses of the system side are re-allocated to the memory chips 1A to 1E in the case of performing swapping according to the rules (1), (2). In this example, after the block address 01 of the memory chip 1A is exchanged with the block address 02 of the memory chip 1B by swapping, the block addresses 01 and 07 in the memory chip 1B are then exchanged with each other by swapping, thereby relocating the block addresses of the system side on the memory chips as shown in the drawing. In this example, looking at the group of the block addresses 01 to 05, the respective block addresses are dispersed and disposed one by

one in the memory chips 1A to 1E. Looking at the group of the block addresses 06 to 10, the respective block addresses are similarly dispersed in the memory chips 1A to 1E. It is thus evident that the initial setting is not broken. Accordingly, the memory management controller 21 of the controller part 2 performs swapping at the physical block addresses of the memory chips 1A to 1E according to the above rules when swapping is needed, whereby the characteristic of reduced time for writing data to the plurality of consecutive block addresses can be kept after swapping.

[0014]

According to the present embodiment, the block addresses of the system side are allocated to the erasure blocks of the memory chips 1A to 1E so that the consecutive block addresses of the system side are disposed extending over the memory chips 1A to 1E the next block being on the next chip; that is, the consecutive block addresses are not allocated in the same memory chip as much as possible, whereby when writing of data extending over the consecutive erasure blocks occurs, the data can be simultaneously written to the consecutive blocks dispersed to the above respective memory chips so that the processing time for writing the data of this type can be reduced. The rules that swapping is performed only among the physical block addresses corresponding to the block addresses of the system side dispersed and allocated to the memory chips 1A to 1E at

the beginning, and that swapping is freely performed among the block addresses in the same memory chip, are provided to thereby keep the form where the consecutive block addresses of the system side are dispersed in the memory chips 1A to 1E even after swapping, whereby the above effect can be prevented from being lessened.

[0015]

[Effect of the Invention]

According to the invention, as described above, the semiconductor filing device can reduce the time required for writing data in the consecutive block addresses of the system side.

Brief Description of the Drawings:

Fig. 1 is a block diagram showing one embodiment of a semiconductor filing apparatus according to the invention; and

Fig. 2 is a diagram showing an example of re-allocating the block addresses of the system side to the erasure blocks of a plurality of memory chips in the case of performing swapping in the apparatus of Fig. 1; and

Fig. 3 is a diagram showing an example of allocating the block addresses of the system side to the erasure blocks of a plurality of memory chips according to the prior art.

[Description of the Reference Numerals and Signs]

1A to 1E: memory chip 2: controller part 21: memory management controller 22: management table

FIGURE 1:

2: CONTROLLER PART 21: MEMORY MANAGEMENT CONTROLLER 22: MANAGEMENT TABLE

1A to 1E: MEMORY CHIP

FIGURE 2:

1A to 1E: MEMORY CHIP

FIGURE 3:

1A to 1C: MEMORY CHIP

AMENDMENT

[Date of Submission] June 18, 1998

[Amendment 1]

[Object of Amendment Document Name] Specification

[Object of Amendment Item Name] Title of the Invention

[Method of Amendment] Change

[Contents of Amendment]

Title of the Invention:

CONTROL METHOD FOR SEMICONDUCTOR MEMORY DEVICE

[Amendment 2]

[Object of Amendment Document Name] Specification

[Object of Amendment Item Name] Claims

[Method of Amendment] Change

[Contents of Amendment]

Claims:

1. A control method for a semiconductor memory device, in which in a semiconductor memory device having a plurality of memory chips to which a plurality of blocks are allocated, to the blocks are designated block addresses of the system side and data is written to the blocks, characterized in that the block address of the system side is converted to the physical block address of the block so that the respective blocks assigned

to the consecutive block addresses of the system side are disposed extending over the plurality of memory chips, the next block being on the next chip.

2. A control method for a semiconductor memory device, in which in a semiconductor memory device having a plurality of memory chips to which a plurality of blocks are allocated, to the blocks are designated block addresses of the system side, data is written to the blocks, and swapping is performed for equalizing the number of times data is written to the respective blocks, characterized in that the block address of the system side is converted to the physical block address of the block so that the respective blocks assigned to the consecutive block addresses of the system side are disposed extending over the plurality of memory the next block being on the next chip, and in swapping between the blocks existing in different memory chips, the swapping is performed only among the physical block addresses corresponding to the consecutive block addresses of the system side disposed extending over the plurality of memory chips one block for each chip.

[Amendment 3]

[Object of Amendment Document Name] Specification

[Object of Amendment Item Name] 0005

[Method of Amendment] Change

[Contents of Amendment]

[0005] It is an object of the invention to overcome the above disadvantage and provide a control method for a semiconductor memory device which may reduce the time required for writing to a semiconductor memory device the data corresponding to the consecutive block addresses of the system side and provide a control method for a semiconductor memory device which may equalize the use frequency of the respective block addresses in a memory module while reducing the time required for writing data.

[Amendment 4]

[Object of Amendment Document Name] Specification

[Object of Amendment Item Name] 0006

[Method of Amendment] Change

[Contents of Amendment]

[0006] According to the invention, in a control method for a semiconductor memory device in which a semiconductor memory device has a plurality of memory chips to each of which a plurality of blocks are allocated and data is written to the blocks when block addresses are designated by a host device, the block addresses of the system side are converted to the physical block addresses of the blocks in such a way that the respective blocks assigned to the consecutive block addresses of the system side are disposed extending over the plurality of memory chips the next block being on the next chip. Further, according to the

invention, in a control method for a semiconductor memory device in which a semiconductor memory device has a plurality of memory chips to each of which a plurality of blocks are allocated and data is written to the blocks when block addresses on the system side are designated, and swapping is performed for equalizing the number if times data is written to the respective blocks, the block address of the system side is converted to the physical block address of the block so that the respective blocks assigned to the consecutive block addresses of the system side are disposed extending over the plurality of memory chips, the next block being on the next chip, and in swapping between the blocks existing in different memory chips, the swapping is performed only at the physical block addresses corresponding to the consecutive block addresses of the host side disposed extending over the plurality of memory chips, the next block being on the next chip.

[Amendment 5]

[Object of Amendment Document Name] Specification

[Object of Amendment Item Name] 0007

[Method of Amendment] Change

[Contents of Amendment]

[0007]

[Operation]

In the control method for the semiconductor memory device

of the invention, the block address of the system is converted to the physical block address of the block of the semiconductor memory device so that the respective blocks of the semiconductor memory device assigned to the consecutive block addresses of the system side are disposed extending over the plurality of memory chips, the next block being on the next chip. In swapping between the blocks existing in different memory chips, the swapping is performed only at the physical block addresses corresponding to the consecutive block addresses of the system side disposed extending over the plurality of memory chips, the next block being on the next chip.

[Amendment 6]

[Object of Amendment Document Name] Specification

[Object of Amendment Item Name] 0015

[Method of Amendment] Change

[Contents of Amendment]

[0015]

[Effect of the Invention]

According to the invention, as described above, in the control method for the semiconductor memory device, the time required for writing data at the consecutive block addresses of the system side can be reduced. While the time for writing data is reduced, the use frequency of the respective block addresses in the memory module can be equalized.